EGC221: Digital Logic Lab

Experiment #6

Hierarchical Logic Circuits Using Intel Quartus Prime

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Assessment:

Assessment Point	**Weight**	**Grade**
Methodology and correctness of results		
Discussion of results		
Participation		
Assessment Points' Grade:		

Comments:

Experiment #6:

Hierarchical Logic Circuit Implementation

Objectives:

The objectives of this experiment are to:

1. implement (and simulate) a 2 x 1 Multiplexer using logic gates,
2. create a (block) symbol of the 2 x 1 Multiplexer, and
3. use block symbols (a hierarchical approach) of the 2 x 1 to implement (and simulate) an 8 x 1 Multiplexer.

Procedure:

Use Intel's Quartus Prime Schematic to solve the following exercises.

Exercise 1:
In this section, a new Quartus® Prime project will be created to design an 8 x 1 Multiplexer circuit, the top-level module. Follow the steps shown in part I of this tutorial to create a new project using **New Project Wizard** in Quartus® Prime.

Choose "**MUX_8x1"** as the name for both the project and the top-level entity. It is important to notice that the name of the top-level entity must match the entity name in the design file.

We will start by designing a 2 x 1 Multiplexer using schematic editor. A Multiplexer uses a control input to select a single data input (from several choices) to be routed to the output of the circuit. If the control SEL is low, then output Y = I_0; else,Y = I_1.

Table 1. Truth table for a 2 x 1 Mux.

SEL	Y
0	I_0
1	I_1

Figure 1 illustrates the block diagram of a 2 x 1 Multiplexer. Design its internal circuit using basic AND and OR gates. Be sure to save as "**MUX_2x1"** and **Set as Top-Level Entity** under the **Projects** pull down menu.

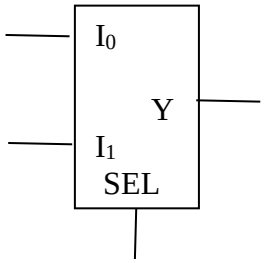

Figure 1. Block diagram of 2 x 1 MUX

(a) Use Quartus Prime Schematic to provide the 2 x 1 Multiplexer circuit diagram

[Insert circuit diagram here]

Figure 2. Quartus Prime circuit diagram of 2 x 1 MUX

(b) Use Quartus Prime Schematic to provide functional verification.

[Insert functional verification timing diagram here]

Figure 3. Quartus Prime functional simulation of 2 x 1 MUX

Exercise 2:

Create a block symbol to represent the above file:

Click inside the ***mux_2x1.bdf*** to make sure this is the active window.

Click ***File -> Create/Update -> Create Symbol Files for Current File.***

Exercise 3:

Create a new schematic diagram file:

Save this file as ***mux_8x1.bdf***

An 8 X 1 Mux has the following truth table.

Table 2. Truth table for an 8 x 1 Mux.

S_2 S_1 S_0	Z
0 0 0	I_0
0 0 1	I_1
0 1 0	I_2
0 1 1	I_3
1 0 0	I_4
1 0 1	I_5
1 1 0	I_6
1 1 1	I_7

Using the Symbol Tool, and under Project you will find your new symbol. Using 2 X 1 Mux's, create the 8 x 1 MUX circuit in Quartus Prime.

Click Project -> Set as Top Level Entity

[Insert circuit diagram here]

Figure 4. Quartus Prime circuit diagram of 8 x 1 MUX

Use Quartus Prime Schematic to provide functional and timing verifications.

[Insert functional verification timing diagram here]

[Insert timing verification timing diagram here]

Figure 5. Quartus Prime simulations of 8 x 1 MUX symbol.
(Functional is shown on top, and timing below)

Download and verify a working 8 x 1 MUX

Conclusions: